CLAIMS

1. An insulated gate field effect transistor, comprising:

a semiconductor body defining opposed first (18) and second (19) major surfaces;

a drain region (2,4) of a first conductivity type extending vertically between the second major surface (19) and part of the first major surface (18);

a body region (6) of a second conductivity type opposite to the first conductivity type extending from the first major surface (18) to a body depth;

a source region (8) of the first conductivity type adjacent to the body region at the first major surface;

a source contact (10) contacting the source region (8) and a drain contact (12) contacting the drain region (2); and

an insulated gate (14) extending laterally over the first major surface over the body region (6), defining a channel region (30) extending in the body region (6) from a source end adjacent to the source region (8) to a drain end adjacent to a drain end part (26) of the drain region (4),

further comprising:

a conductive shield plate (22) for shielding the gate, extending in an insulated trench (20) from the first major surface (18) towards the second major surface (19), the conductive shield plate being separated from the body region (6) by part of the drain region (4) including the channel end part (26) of the drain region.

2. An insulated gate field effect transistor according to claim 1, further comprising a conductive shield plate extension (32) connected to the shield plate (22) extending laterally over the first major surface (18) of the drain region (4) from the shield plate (22) towards the channel end part (26) of the drain region (4), the shield plate extension being separated by insulator (16) from the drain region (4).

3. An insulated gate field effect transistor according to claim 2, wherein a gate insulator (16) layer extends under both the gate (14) and the shield plate extension (32).

4. An insulated gate field effect transistor according to claim 2 or 3 wherein the lateral gap between shield plate extension (32) and gate (14) is in the range 0.05 to 0.2 micron.

5. An insulated gate field effect transistor according to any preceding claim wherein the shield plate (22) is connected to the source (8).

6. An insulated gate field effect transistor according to any preceding claim wherein the depth of the shield plate trench (20) is between 50% and 200% of the depth of the body region (6).

7. An insulated gate field effect transistor according to any preceding claim, wherein the first conductivity type is n-type, the second conductivity type is p-type, and the shield plate (22) is of p-type doped polysilicon.

8. An insulated gate field effect transistor according to any preceding claim, wherein the lateral gap between the shield plate trench (20) and the body region (6) is between 0.5 and 2 microns.

9. An insulated gate field effect transistor according to any preceding claim, wherein the gate (14) extends over the channel end part (26) of the drift region by no more than 0.4 micron.